Electron Transport in InAs-InAlAs Core-Shell Nanowires

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Evidence is given for the effectiveness of InAs surface passivation by the growth of an epitaxial $In_{0.8}Al_{0.2}As$ shell. The electron mobility is measured as a function of temperature for both core-shell and unpassivated nanowires, with the core-shell nanowires showing a monotonic increase in mobility as temperature is lowered, in contrast to a turnover in mobility seen for the unpassivated nanowires. We argue that this signifies a reduction in low temperature ionized impurity scattering for the passivated nanowires, implying a reduction in surface states.

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I. INTRODUCTION

InAs nanowires are a promising material for use in nanoscale circuits[1], single electron charge sensing[2,3], and infrared optoelectronics applications[4], and due to a large spin-orbit interaction, are of potential interest for spin-based[5] and topological[6] quantum information processing. The intrinsic donor-like surface states of InAs play a major role in determining transport properties[7], and lead to reduced electron mobilities at low temperatures due to ionized impurity scattering[8]. The charged surface states produce a random spatial electrostatic potential in the nanowire, which may contribute to the spontaneous formation of quantum dots at low temperature[9]. These states can also quench intrinsic photoluminescence, severely limiting the performance of optoelectronic devices[4,10]. Surface passivation should reduce the density of ionized surface states and lead to improved electron mobility. Growth of an InP shell on an InAs core[11] has been shown to yield better mobilities, as well as chemical passivation based on In-S bonding[10,12,13]. Here we study the effects of surface passivation due to an epitaxial $In_{0.8}Al_{0.2}As$ shell, which is predicted to give a so-called type I heterostructure[14] in which both electrons and holes are confined to the InAs core. The bandgap of $In_{0.8}Al_{0.2}As$ should be 0.41 eV larger than that of InAs[15] for an unstrained zincblende structure, however our nanowires are wurtzite and strain is likely to modify the bandgaps somewhat[14]. We note that the lattice mismatch to InAs is smaller for $In_{0.8}Al_{0.2}As$ shells compared to InP shells, which should result in less interfacial strain and the ability to grow thicker shells free of dislocations. We performed transport measurements on core-shell nanowire field-effect transistors (FETs) at temperatures ranging from 1-200 K. By comparing with transport results on pure InAs nanowires grown under nominally identical conditions, we obtain clear evidence for the reduction of ionized impurity scattering in the core-shell nanowires, leading to the highest mobility we have yet observed in an InAs FET device at low temperature. These results show that InAlAs epitaxial shells have the potential to significantly improve the quality of nanoelectronic devices based on InAs nanowires.

II. NANOWIRE STRUCTURE

Core-shell nanowires were grown in a gas source molecular beam epitaxy system using Au seed particles[16]. First, InAs cores were grown axially by the Au assisted vapour liq-
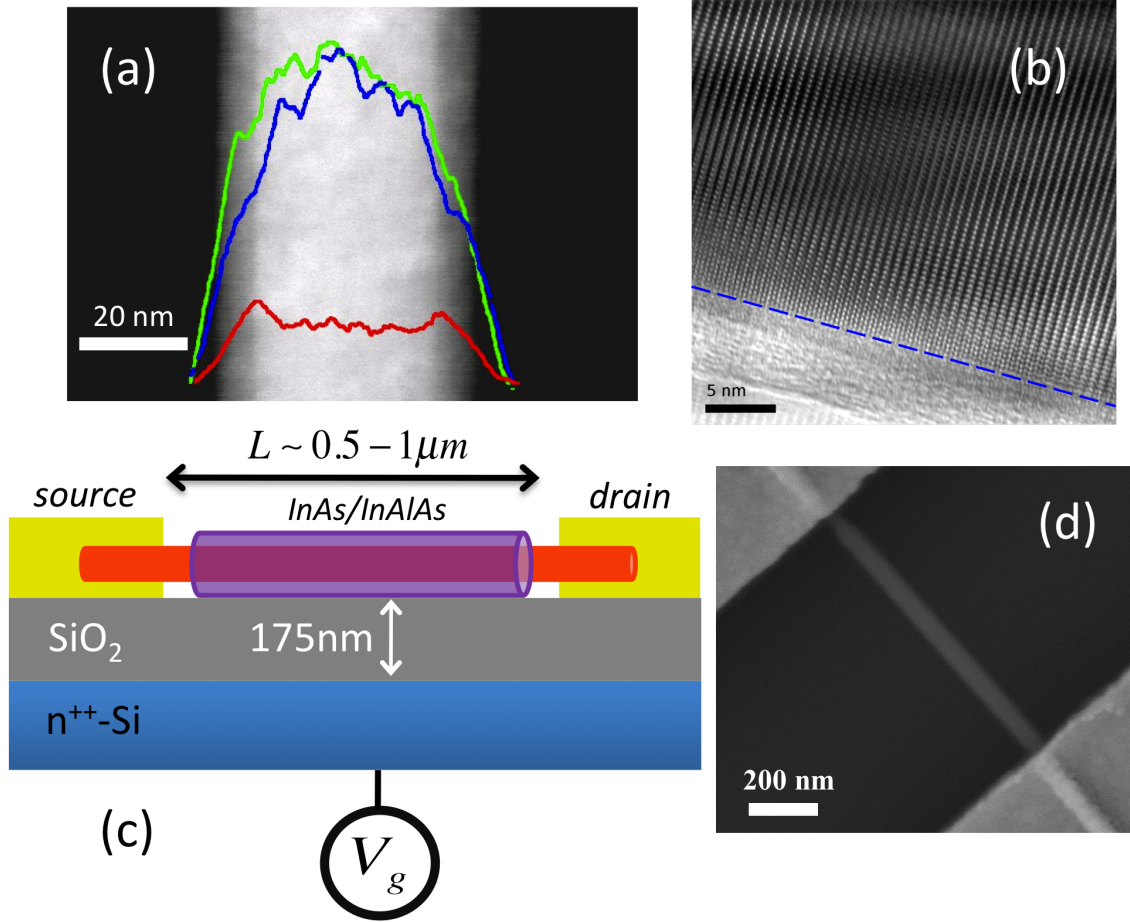
FIG. 1. (a) High-angle annular dark field image of InAs - $In_{0.8}Al_{0.2}As$ core-shell nanowire with superimposed energy-dispersive x-ray spectroscopy linescan (Al: red, In: blue, As: green). (b) High-resolution TEM image taken along the $[2\bar{1}\bar{1}0]$ zone axis, showing an absence of dislocations in the shell. The dashed line indicates the nanowire surface. (c) Schematic cross-section of the FET device. (d) SEM image of device 3. The etching profile of the nanowire is seen near the metal contact at the upper left.

uid solid mechanism on a p-GaAs (111)B substrate at a growth temperature of 420 °C. This was followed by the inclusion of Al to facilitate radial growth of the $In_{0.8}Al_{0.2}As$ shell[17].The nanowires were characterized using transmission electron microscopy (TEM). As-grown nanowires were sonicated and suspended in ethanol, dispersed onto TEM grids with holey carbon films, and imaged with a JEOL 2010F TEM with an accelerating voltage of 200 kV. Low-magnification TEM images of typical nanowires reveal that the nanowires

have an inner core and an outer shell structure. In general, the nanowires had a core diameter of 20-50 nm and a shell that was 12-15 nm thick, independent of core diameter. The chemical composition of the nanowires was analyzed by energy-dispersive x-ray spectroscopy (EDS). As shown in Figure 1a, the EDS line scan analysis along the radial direction shows In and As in the core region and In, As and Al in the shell region. High-resolution TEM (HRTEM) image of a representative unetched nanowire in Figure 1b clearly shows lattice fringes of a single-crystal nanowire along the $[2\bar{1}\bar{1}0]$ zone axis. Both core and shell exhibit wurtzite crystal structure, evidenced by ABAB... stacking, and confirmed by selected area diffraction. HRTEM and electron diffraction data are both consistent with a dislocation-free core-shell interface for these nanowires. However, at higher Al concentrations, dislocations due to relaxation of the core-shell interface are observed[17]. The nanowires studied here had low stacking fault densities, achieved by using sufficiently low growth rates[17,18]. Below, we also show data from unpassivated InAs nanowires that were grown under nominally identical conditions to the growths of the nanowire cores mentioned previously, except that the axial growth rate was 0.25 μm/hr and 0.5 μm/hr for the core-shell and bare nanowires, respectively.

III.   FIELD-EFFECT TRANSISTORS

FET devices were fabricated using a standard e-beam lithography technique. As-grown nanowires were mechanically deposited onto a 175 nm thick SiO_2 layer above a n^{++}-Si substrate. Selected nanowires with diameters $40-80$nm were located relative to pre-existing fiducial markers by scanning electron microscopy (SEM), with care taken to minimize the electron dose. The contact areas were etched with citric acid to remove the shell material, followed by room temperature sulfur passivation to prevent oxide regrowth[19] during the sample transfer to an e-beam metal evaporator. Ni/Au (30nm/50nm) metal contacts were deposited and annealed at 120 °C in vacuum for 5 minutes to promote Ni diffusion into the nanowire contact area[20]. The device structure is shown schematically in Fig. 1c, and a SEM image of a representative device is shown in Fig. 1d. After fabrication the device chip was wire-bonded into a chip carrier and transport measurements were carried out in either a continuous flow He cryostat operating from 4-200 K or a dilution refrigerator allowed to slowly warm from 1.2 K. Upon applying a DC source-drain voltage V_{sd}, the device current
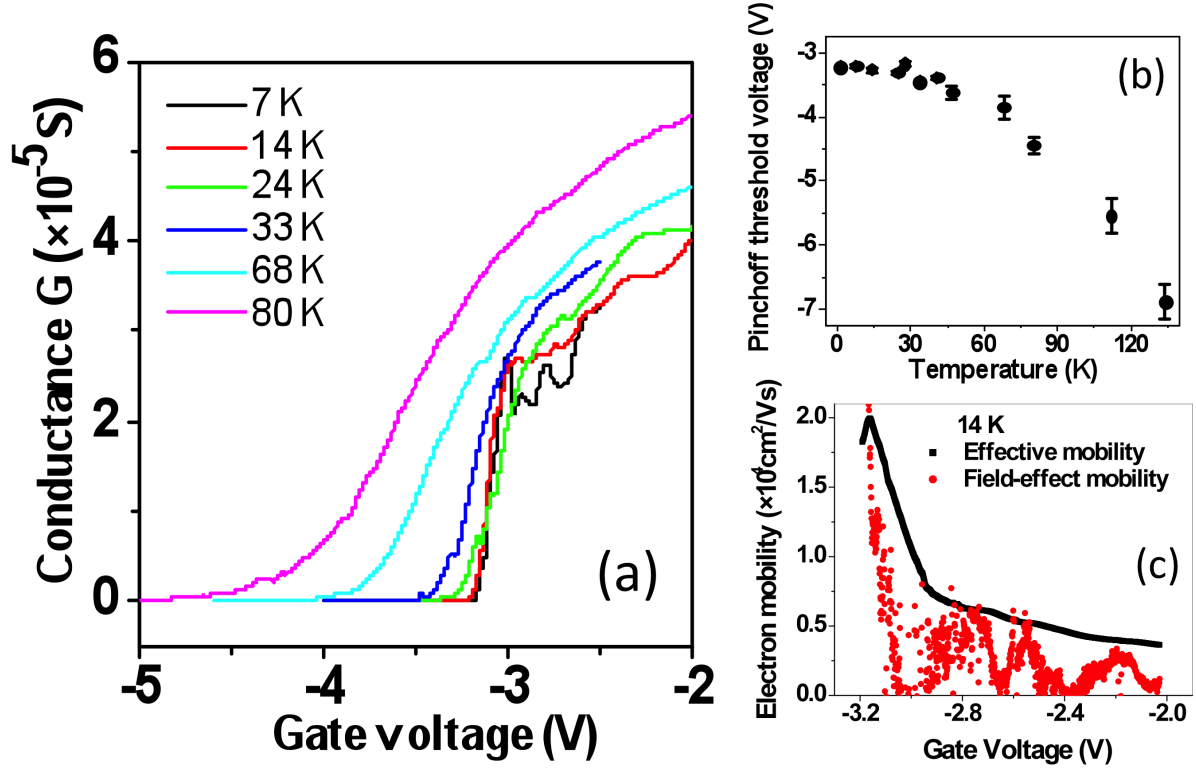
FIG. 2. (a) Conductance versus backgate voltage for core-shell nanowire FET device 1, at various temperatures. (b) Pinchoff threshold voltage as a function of temperature for device 1. (c) Field-effect (red dots) and effective (black squares) mobility versus backgate voltage for device 1 at $T = 14$ K. The effective mobility remains a smooth function despite the oscillations in conductance that appear at low temperatures.

I_{sd} was measured using a current-voltage preamplifier at a 3 Hz bandwidth. A separate voltage V_g applied to the degenerately doped Si substrate provided a global backgate.

IV. TRANSPORT MEASUREMENTS

Many devices have been investigated to different levels of detail, but here we will focus on results from three core-shell nanowire FETs (devices 1-3) and three pure InAs nanowire FETs (devices 4-6) for which detailed mobility analysis was performed. Pinchoff threshold data from additional core-shell devices is also included in Fig. 3. Devices 1-3 had total diameters 80 nm, 75 nm, and 51 nm, respectively, measured after transport measurements by SEM

at a magnification of 100k, with uncertainties ± 2 nm. These correspond to core diameters of roughly 54 nm, 49 nm and 25 nm, respectively. The FET channel lengths were 465 nm, 465 nm, and 940 nm, respectively. Figure 2a shows selected conductance $G = I_{sd}/V_{sd}$ versus backgate curves for device 1. As temperature is lowered, the device 'on' conductance decreases due to decreasing carrier density, but the field-effect mobility increases, indicated by the increasing slope $\frac{dG}{dV_g}$ near conductance pinchoff. Pinchoff threshold voltages V_T, shown in Fig. 2b versus temperature, are determined by the $G = 0$ intercept of the line tangent to the maximum slope in conductance. V_T shifts to more negative values with increasing temperature; this can be understood by the thermal activity of surface donor states causing the downward band bending at the surface to increase, leading to a larger accumulation of carriers at the surface and requiring larger negative gate voltages to reach pinchoff.

The field-effect and effective mobilities, μ_{fe} and μ_{eff}, are deduced from the conductance data using two different analytical expressions:

$$\mu_{\mathrm{fe}} = \frac{L}{C'_g} \frac{dG}{dV_g} \tag{1}$$

$$\mu_{\mathrm{eff}} = \frac{L}{C'_g} \frac{G}{(V_g - V_T)} \tag{2}$$

Here, L is the channel length, V_g is the gate voltage, V_T is the threshold voltage, and C'_g is the gate capacitance per unit length. C'_g is estimated as the capacitance of a wire above an infinite conducting plane in series with the cylindrical capacitance between the core and shell. In estimating C'_g, we take into account that the nanowire is not embedded in the SiO_2 dielectric[21]. The field-effect mobility is strictly only valid at the peak mobility where $\frac{d\mu}{dV_g} = 0$, and it is generally a lower bound on the effective mobility. Figure 2c shows the comparison of the field-effect and effective mobilities for device 1 at T = 14 K. The effective mobility is typically a smoother function of V_g than the field-effect mobility, and $\mu_{\mathrm{eff}} \geq \mu_{\mathrm{fe}}$ within experimental error for all our data. In the following, we take the effective mobility as our preferred measure. Two regimes of μ_{eff} are seen with respect to gate voltage in Fig. 2c, with a sharp rise in mobility near pinchoff, in contrast to a slowly varying mobility at more positive gate voltages. The decrease in mobility as the device is turned on is understood by the increase in inter-subband scattering as more radial subbands are filled[22], and a larger carrier density near the surface.

In figure 3, we compare the peak effective mobilities of the core-shell and pure InAs nanowires across a wide temperature range. The unpassivated InAs devices 4-6 had di-

ameters 71 nm, 50 nm, and 35 nm, respectively, with uncertainties ±2 nm. The channel lengths were 2.95 μm, 970 nm and 770 nm respectively. Only the unpassivated devices exhibit a turnover at low temperatures, where mobility rapidly decreases with decreasing temperature. In contrast, the mobilities of the core-shell nanowires increase monotonically as temperature is lowered, even down to $T = 1$ K (effective mobility could not be properly measured below 1 K due to the onset of strong Coulomb blockade). The turnover in mobility for the unpassivated nanowires occurs between 25 and 45 K. We have investigated several more specimens of both nanowire types, and see a similar turnover in mobility only for the unpassivated nanowires. The data in Fig. 3 have been fit to empirical power law expressions to guide the eye. The fits for the unpassivated nanowires are of the form $\mu_{\text{eff}} = (\frac{1}{\alpha T^a} + \frac{1}{\beta T^b})^{-1}$, based on combining mobilities from two scattering mechanisms using Matthiesen's rule. The fits for the core-shell nanowires are single power law functions, $\mu_{\text{eff}} = \gamma T^c$. The temperature power law exponent describing the negative slope region for the pure InAs nanowires varies from -0.5 to -1.5, whereas it varies from -0.3 to -0.7 for the core-shell devices. We note that the highest core-shell nanowire mobility observed was $\approx 25,000$ cm^{2}V^{-1}s^{-1} at 1 K for device 1 (core diameter ~ 50 nm), higher than the peak mobility $\approx 20,000$ cm^{2}V^{-1}s^{-1} at 35 K for the unpassivated device 4 (diameter ~ 70 nm). The latter was the highest mobility we observed in MBE-grown InAs nanowires prior to investigating the core-shell nanowires. Mobilities in excess of 20,000 cm^{2}V^{-1}s^{-1} have also been observed with InAs-InP core-shell nanowires[11] at low temperature.

V. DISCUSSION

To explain the results above, we must first consider the possible scattering mechanisms for conduction electrons in InAs nanowires. Acoustic phonon scattering can be ruled out as the limiting mechanism, because it would yield much higher mobilities $\sim 5 \times 10^6$ cm^{2}V^{-1}s^{-1} at room temperature[23]. Similarly, optical phonon scattering is only expected to dominate at much higher temperatures[23]. Surface roughness and ionized impurity scattering are the most plausible mechanisms. Although we cannot strictly rule out the presence of bulk impurities, we expect the densities to be very low in comparison to the density of surface states. The presence of these donor-like surface states[7,12] at a density of $10^{11} - 10^{12}$ cm^{-2}, together with the large surface-to-volume ratio inherent to the nanowire geometry, suggests
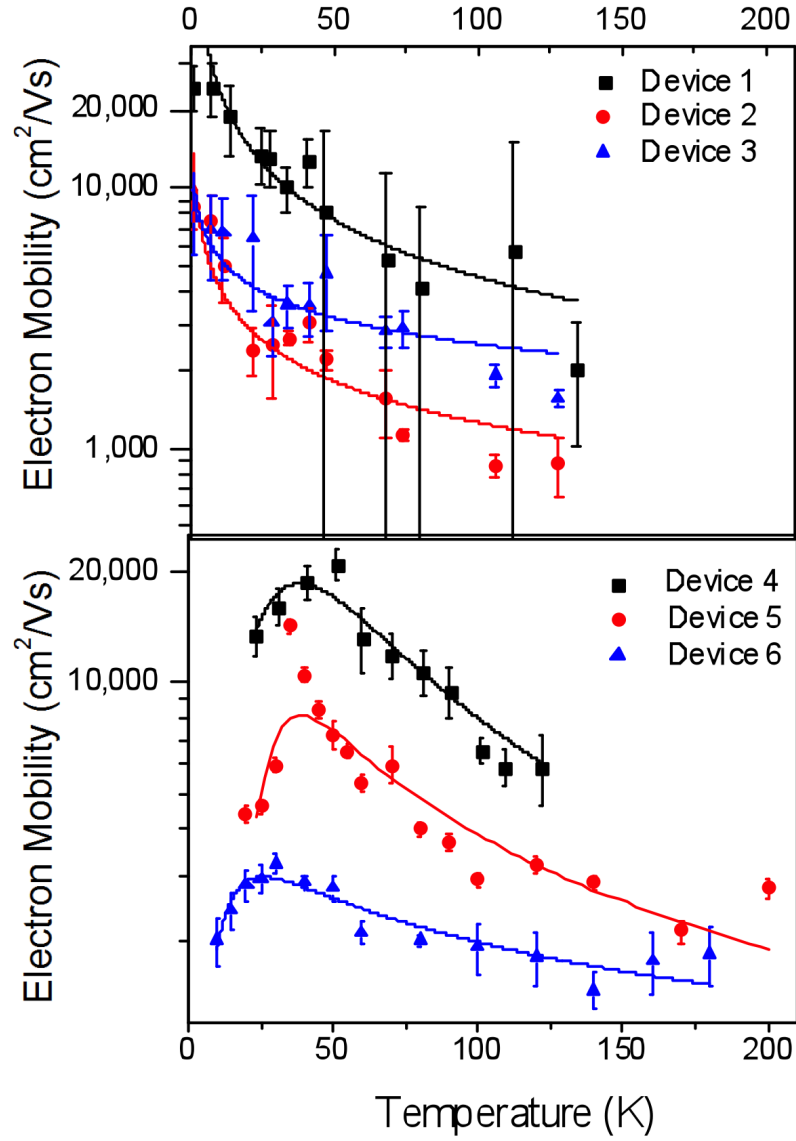
FIG. 3. Peak effective electron mobility versus temperature for core-shell devices 1-3 (upper panel) and unpassivated devices 4-6 (lower panel). The empirical fits, based on power laws, are described in the text. On average, mobility increases with nanowire diameter, as is seen here for the unpassivated nanowires.

that scattering at the surface is most likely dominant. This is consistent with the diameter dependence seen in Fig. 3; the mobility generally increases with diameter both for the core-shell and unpassivated nanowire devices, similar to previous reports[24].

The downturn in mobility at low temperatures for the pure InAs nanowires is consistent with ionized impurity scattering[23]; the scattering rate increases as the electron Fermi velocity

decreases at lower temperatures. Surface roughness scattering could produce a similar trend, but is less likely to limit the mobility to values as low as we observe. On the other hand, how can we understand the negative slope of μ_{eff} versus T for the core-shell nanowires and for the pure nanowires above ~ 45 K? We suggest this can be understood by the change in surface state scattering rate as the conduction electron concentration and radial distribution change with temperature. At low temperature, the lowest radial subband is primarily occupied, whose wavefunction has a relatively small overlap with the surface, leading to a relatively high mobility. As temperature increases, higher radial subbands are occupied and the total carrier concentration increases, leading to a greater fraction of electrons near the surface, enhanced by the negative surface band bending[25]. This lowers the mobility, or increases the scattering rate, because electrons are closer on average to the scattering centers, and also more electron states become available for intersubband scattering[22]. The increase in carrier concentration with temperature is consistent with the observed shifts in pinchoff threshold voltage, an example of which is shown in Fig. 2b. This also suggests that the density of ionized states at the surface increases with temperature (to donate the electrons), which will also increase the scattering rate. On the other hand, if a sufficient density of ionized surface states are frozen in at low temperature, and the conduction electrons only occupy the lowest subband, then the mobility should turn over and exhibit a positive slope due to the simple dependence of scattering probability on the Fermi velocity $\propto \sqrt{T}$. We hypothesize that the absence of a turnover in mobility for the core-shell nanowires indicates that the density of frozen-in ionized surface states is significantly reduced by the shell passivation. A detailed calculation of surface scattering rates as a function of thermal subband occupation will be carried out in future work.

VI. CONCLUSION

We have shown evidence through electron transport for the effectiveness of an $In_{0.8}Al_{0.2}As$ shell to passivate the InAs nanowire surface. Our data suggests that the density of ionized surface states at low temperature is significantly reduced in core-shell nanowires compared to unpassivated nanowires. Further support for this hypothesis could be gained by mid-infrared photoluminescence (PL) studies that show removal of surface states upon passivation[10]. These core-shell nanowires are expected to offer new opportunities to realize

high quality devices for quantum transport and optoelectronics applications.

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